WHITE PAPER

An SDR Platform for Satellite Earth Stations

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Abstract

Satellite communication continues to grow in the burgeoning Wireless marketplace. Be
standard Wireless telecommunications drivers such as ubiquitous high-speed communic
Internet access, satellite communication demand is also driven by entertainment applica
direct and interactive television.

The demands imposed by the increase in satellite communication traffic drive the requir
improvements in satellite network infrastructure equipment. The equipment must hand
channel densities and must meet a high-availability standard to provide uninterrupted s
addition, it is desirable that this equipment be flexible to accommodate various air
protocols. As is the case with other forms of wireless communications, digital signal proc
the means to achieve these performance goals.

In the past, custom digital circuitry was required to implement digital signal processing e
Today, however, digital technology is sufficiently powerful to enable the applic
Commercial-Off-The-Shelf (COTS) technology to these challenges in the form of software
radios (SDRs). By employing this COTS approach, the infrastructure Original E
Manufacturers (OEMs) can focus their efforts on higher system-level features and differe
while realizing the cost and resource benefits from outsourcing the radio signal pr
portion.

This paper discusses the elements of modern satellite earth stations and describe
combination of Digital Signal Processors (DSPs), Field Programmable Gate Arrays (FP
commercially available communications Application Specific Integrated Circuits (ASICs
implemented to build an SDR platform for these elements. Practical examples of COTS
that can be used to realize this solution are presented.

Introduction

Satellites communication (satcom) has unique features that make it an interesting part
the telecom arena. This uniqueness arises from satcom's ability to fill roles currently p
both terrestrial wireless and wireline networks. Today, this is seen by the application of sa

- Broadband enterprise networks, where multiple remote sites of a company are c
  with high-speed data networks
- Home and enterprise broadband internet access
- Fixed telephony, where satellite telephony stations are set up in locations that
  terrestrial telecom infrastructure either due to geographical obstacles or economic
- Mobile telephony and data access, where satellite systems are just now beginnin
  global wireless access to compete with the local terrestrial cellular and PCS syste

The first three applications listed above are instances where satcom is used in place
wireline networks; the last is an example of its ability to address wireless applications.

To fill its roles in these areas, new satellite network infrastructure equipment must hand
channel densities and meet a high-availability standard to provide uninterrupted servic

signal processing is the means to achieve these performance goals.

This article, will briefly review some of the different types of commercial satellite systems in use or in development and some of the common elements of Earth Stations. It will des concept of Software Defined Radio (SDR) and how it is realized today using a combi Commercial Off-The-Shelf (COTS) Digital Signal Processors (DSPs), Field Programma Arrays (FPGAs) and commercially available Application Specific Integrated Circuits (ASIO then describe how these SDR elements can be applied to the Earth Stations, using exa actual COTS equipment. Finally, it will discuss some of the challenges that remain in SDR solutions to Earth Stations, and some potential solutions.

Satellite Earth Stations

When categorized by orbits, satellite systems can fall into one of four general categories
- ☐   HEO, or highly elliptical orbits, orbiting at any altitude but with a non-circular orbit
- ☐   LEO, or low earth orbit, orbiting at an altitude between 700km and 1400km
- ☐   MEO, or medium earth orbit, orbiting at an altitude between 10,000km and 15,000
- ☐   GEO, or geostationary earth orbit, orbiting the equator at an altitude of 36,000km

Examples of existing and planned systems of GEO, MEO, and LEO systems are shown
1.

Orbit	Company/System	Primary Function	ISL* / Bent Pipe**	Exists / Developing
GEO	Hughes/DirecPC	Broadband internet	Bent Pipe	Exists
	Hughes/Personal Earth Station	Enterprise VSAT***	Bent Pipe	Exists
	Gilat/Skystar Advantage	Enterprise VSAT	Bent Pipe	Exists
	Gilat/Starband	Broadband internet	Bent Pipe	Exists
MEO	New ICO	Mobile phone/data	Bent Pipe	Developing
LEO	Iridium	Mobile phone/data	ISL	Exists
	Globalstar	Mobile phone	Bent Pipe	Exists
	Teledesic	Broadband internet	ISL	Developing

Table 1: Examples of satellite systems. Sources were [2], [3], [4], [5], [6].

*ISL = inter-satellite links – direct communication channels between satellites, not involving earth stations
**Bent Pipe = satellite simply acts as a re-transmitter – signals sent from a ground-based transmitter are redirected to a ground-based receiver without undergoing any modification to the payload
***VSAT = Very Small Aperture Terminals (typically under 2m in diameter)

The type of orbits and frequencies used influence the nature of the communications sys instance, latency is significant in GEO systems because of the sheer distance involve 120ms one-way trip to satellite). On the other hand, LEO systems must contend with correction due to the high relative speed of the satellites, as well as frequent (every 20 maximum [15]) inter-satellite hand-over as they move out of the range of terminals a stations. To reach higher data rates, newer systems are progressing to higher frequen such as the Ka-band (18-31Ghz), where the signals are susceptible to significant atm attenuation. [15]

Although the differences in the 3 types of satellite systems have significant affects o aspects of the design of and number of earth stations, other portions of the statio architecturally common. **Figure 1** illustrates some of the key elements in an earth station

Note that for the air interface, Globalstar and a few other systems use a CDMA (code multiple access) protocol, but the majority of systems use a hybrid combination of f and/or time division multiplexing and multiple access on the downlink and uplink, respect
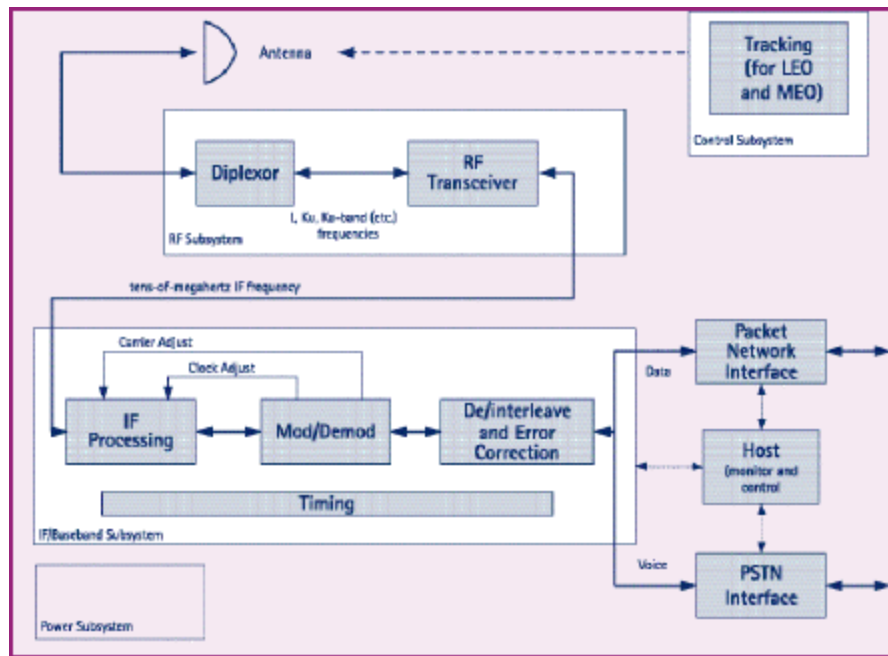
Figure 1

By the way, in case you have wondered about the difference between multiplexing an
access (e.g., like TDM vs, TDMA), here is the answer you seek. Multiplexing takes place
plans for sharing the communications resource are known in advance, such as the case
earth station (a single source) sends multiple channels of communications out
transmission. Multiple access occurs when multiple remote entities must share the re
such as a bunch of user terminals trying to send data back to the earth station via satellit

Before we can describe how digital technology can handle the problem of earth station p
requirements, we need to discuss the concept of software defined radio.

Software Defined Radio (SDR)
The essence of SDR is, as the name would imply, the idea of processing radio sig
combination of software and firmware, rather than relying primarily on fixed-function A
Specific Integrated Circuits (ASICs) or analog components. The motivation to pursue a
based approach to radio signal processing is similar to that driving the application of s
other endeavours:

  □ Flexibility to evolve modulation/air-interface algorithms and protocols by uploac
     software onto the same hardware
  □ Adaptable systems that can adjust capability on-the-fly as network or traffic c
     change (e.g., as more data versus voice users come online, processing can be d
     accommodate)
  □ Realize economies of scale by using a common hardware platform across variou
     applications and loading it with the appropriate application software (e.g., commor
     for Mobile Telephony systems, Fixed telephony/data systems, Broadband
     systems, enterprise VSAT)

The flexibility of SDR implementations is particularly convenient for bent-pipe architectur
that do not use on-board processing (OBP), since changes in Earth Stations do not re
corresponding adjustment to algorithms in the satellite payload.With today's processor te
the goal of performing all of the processing in software is still not achievable. Howeve
being realized today using a combination of software running on processors, firmware r
FPGAs, and some programmable ASICs, specific examples of which are discussed ir
section.

Processors

Processors such as Texas Instruments' C6000 DSP family are well suited for p
elements of the modem and higher layer protocol functionality in SDR systems as
decision-type processing. In addition, they can perform monitoring functions, such as ca
received SNR, Eb/No, and bit error rates. The processors are designed to operate on
data streams and are equipped with multiple buses, interleaved memory banks, a
engines. They are programmable in Assembly language or C, and come with advanc
building and debugging environments to ease the code development task.

The current members of this processor family are all based on the same core architectu
multiple execution units operate on multiple program instructions at the same time. Th
C6202, and C6203 are the current generation of fixed-point processor in this family, ru
200 MHz, 250 MHz, and 300 MHz, respectively. These 3 processors are functionally quit
differing mainly in power, package size, clock speed, amount of internal memory (increas
some of the peripheral architecture (e.g., number of serial ports, secondary bus charac
The 'C6701 is the pin-compatible floating-point counterpart of the C6201, running at 167

The next generation of the C6000 fixed-point family is the C64x series. The C6416 is th
performance model in this generation, coming out initially at 600 MHz, with a roadma
GHz. The C6416 also includes special hardware and instruction features for turbo, Vit
Reed-Solomon en/decoding, bit interleaving and de-interleaving, etc., resulting in perf
improvements exceeding those provided by clock speed increase and core arc
enhancements alone. [8]

FPGAs

While processors offer the flexibility of easy programmability, they are still inherently limit
sequential execution paradigm that they follow.[1] For algorithms that can operate in pa
multiple inputs, the FPGA, despite operating at clock speeds significantly less than D
provide substantial throughput gains. Examples of such algorithms are FIR filters, error c
coding and decoding algorithms (e.g., turbo codes, convolutional codes), correlators (e.
spreading spread-spectrum signals), etc. By configuring the logic elements of th
numerous multiply-and-accumulate operations can occur in a single cycle, compared t
where typically only one or two occur in a single cycle. Today, FPGAs such as the Xili
series provide up to one million logic gates (XCV400- 400K gates, XCV1000 = 1 milli
etc.) grouped into logic blocks, (and RAM) that can be configured by users to create th
logic, FIFOs, etc. The FPGAs also have a large number of I/O pins, permitting
throughput. The next generation of Xilinx FPGAs (Virtex II) comes in sizes up to 10 milli
and include internal multipliers to enhance performance even further.

The tradeoff for all of this wonderful power is significant added complexity in the tools
building process. It is no longer a straightforward matter of writing code, compiling it, dov
and executing it. The code is more difficult to write, especially if decision structures
machines are required to create more complex conditional logic. Additionally, the designs
simulated, and then routed and placed onto the FPGA matrix. At higher speeds, rou
placement choices can introduce timing issues that can cause designs to fail o
inconsistently a class of problems not seen in the DSP environment.

ASICs

Although FPGAs and processors are catching up, ASICs still provide the ultimate in term
power consumption, smallest package size, cheapest cost per unit, and highest perf
What counter-balances this "ultimateness"? The power consumption and size aspects
relevant in the portable equipment applications, the cheap unit cost comes at the exper
greatest upfront investment, and the high performance comes with limited flexibility if yo
change to the protocol or algorithm, you must create a new ASIC.

In SDR systems, ASICs play a role at the digital up and down conversion stag
downconverters like the Graychip GC4016 and Intersil 50214B are responsible for impl
the IF-to-baseband down conversion and decimation. The chips have digital NCOs,
remove aliases resulting from decimation, re-samplers (some models) and a variety of I/

for synchronization and control. Some, like the Graychip GC1012 are dedicated to
down conversion, having a minimum decimation of 2; others, like the Graychip 4016 ca
the-fly re-configured as either four narrowband downconverters, each with a maximum
baseband bandwidth of 2.25 MHz per channel, or as a single channel wideband down
with a maximum useable baseband bandwidth of 9 MHz [9]. ASICs like the Graychip GC
Intersil HSP50215 provide similar functionality on the upconversion side.

Applying SDR to Satellite Earth Stations

Today, SDR solutions apply to the IF/Baseband (modem) subsystem portion of **Figu**
introduction of digital or software defined radio into terrestrial cellular base transceiver
(BTSs) has generally been done using proprietary technologies, ASICs, and so forth. I
for satellite infrastructure equipment, the use of COTS (Commercial-Off-The-Shelf) ec
based on standard backplanes, DSPs, FPGAs, and (fewer) specialized ASICs, see
appropriate. This suitability stems from several factors, among them:

1. DSP and FPGA technology have reached a sufficient state of maturity/complexi
    implementation of SDR algorithms. This was not the case some years ago, wh
    cellular base station manufacturers began developing the SDR portions of their BT

2. The added complexity of satellite-based systems. This is especially evident in th
    LEO systems that must deal with tracking, Doppler correction, and "mov
    stations" (i.e., handoff between satellites required as they themselves move out
    not only when terminals move). These systems would benefit from SDR flexibilit
    system performance during roll-out.

3. The number of satellite earth stations is substantially less than the number o
    BTSs. Under this reduced volume, COTS solutions can be more cost effect
    pursuing an ASIC-based solution that generally requires large production quanti
    which to amortize the initial investment.

Note that the following discussion will focus on the receive-side of the base station, alth
transmit-side would follow similarly, using corresponding upconverter ASIC modules
modules.

Although it may vary, one method for partitioning the modem functionality between th
FPGAs and DSPs is the following:

The ASICs are used for the IF to baseband downconversion (i.e., mixing with an
decimation of the data stream. Carrier frequency corrections may also be fed back to t
from processing that occurs further downstream in the FPGA or DSP.

Equalization filters, demodulation (including chip-rate de-spreading of spread-
modulation schemes such as CDMA), frame buffering, carrier, symbol, and fram
extraction are implemented in the FPGA. De-interleaving and FEC (channel) decoding
be done here.

In the DSP, FEC decoding, de-multiplexing and de-interleaving of frame data, decryp
source decoding, physical layer power control loops, and other physical layer protoco
(e.g., hopping sequence for combination FDMA/TDMA protocols) can take place. As well
tuning of parameters from algorithms executed in the FPGA and ASIC can be controlled
DSP.

To implement this SDR solution today, various architectures based on COTS boards
considered. In the following paragraphs, we discuss some example architectures c
equipment that can be used to implement the IF/baseband portion of the Earth Station.

Fully COTS Solution

Figure 2 illustrates a COTS SDR system. The system consists of a hot-swap CompactP processing baseboard having the ability to carry mezzanine modules that contain A/D c (labeled PMC-2MAI) and digital downconverters (labeled PEM-16MSDDC).
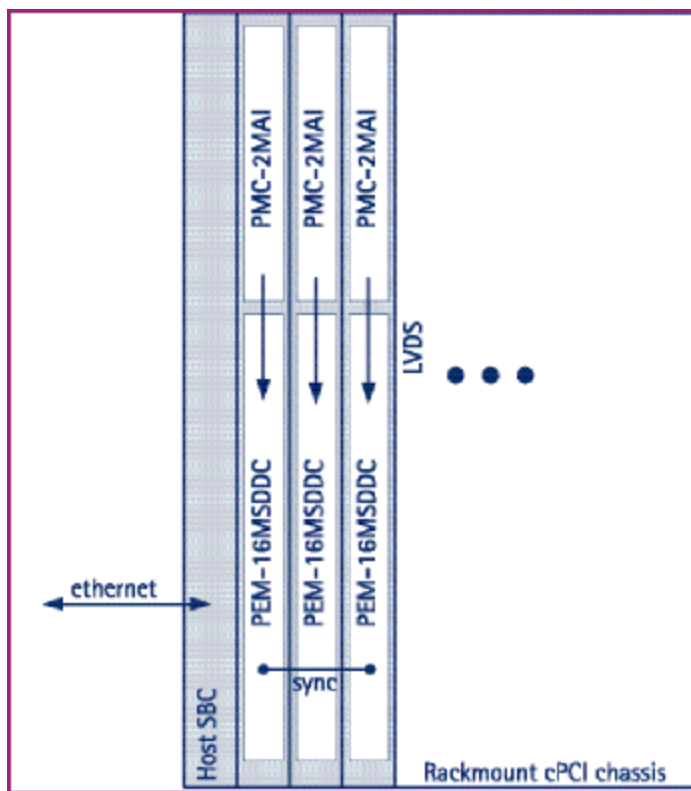

Figure 2: COTS SDR System

Figure 3 contains an actual photo of a cPCI processing baseboard and highlights mezzanine module locations. The PCI Mezzanine Card (PMC) site on the left provides c to the board's local PCI bus through the connectors in the upper left corner of the phot where the PMC-2MAI sits. The Processor Expansion Module (PEM) site on the right individual connections directly to each DSP's external memory bus using the fou connectors in the lower right corner of the photo. This is where the PEM-16MSDDC sits.
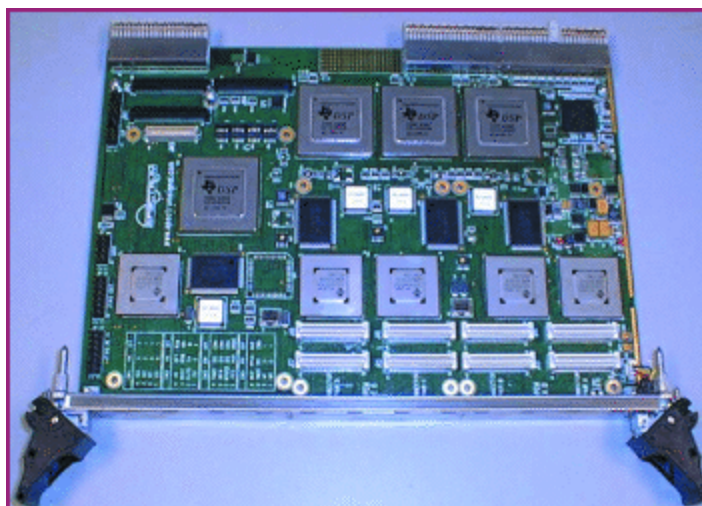

Figure 3: Example of a COTS board for SDR

In **Figure 2**, the SDR system begins at the A/D converter, where the analog IF signal is

and sent over a lowvoltage differential signaling (LVDS) bus to the downconverter mezz the PEM sites of several processing baseboards. LVDS is a robust method for send frequency signals over distance by cable. Each PEM module has 4 digital downconvert as well as some FPGAs. The digitized data from the A/D flows is downconverted and d in the downconverter ASICs. The output from each ASIC flows into an FPGA, where further processed before flowing into one of the DSPs. In the case where each of downconverter ASICs is the Graychip 4016 discussed previously, the PEM mo downconvert up to 16 narrowband frequency or 4 wideband channels. In other words, board can be working on up to 16 narrowband or 4 wideband frequency multiplexed each of which may in turn consist of several time-multiplexed channels. Up to six pr baseboards can be cascaded from the LVDS bus carrying the digitized IF outputs from e giving the capability to handle up to 96 narrowband (or 24 wideband) frequency chann processors.

Of course, depending on the channel bandwidths/data rates involved, it may not be p handle 4 channels per DSP-plus-FPGA unit. In this case, multiple DDCs could be tun same center frequency, allowing several DSPs and FPGAs to split the burden of frequency channel (e.g., parsing different time slots from within the TDM frame for that frequency channel). This also permits the flexibility to adapt to changing network traffic by dedicating more processors to bear on channels that are particularly busy, by pulling of other channels (e.g., to allocate to channels whose TDM slots are filled). All of thi controlled by software, since the DDCs center frequencies can be changed on-the-fly, i one of the key flexibility elements possible with SDR systems.

Once data has passed through the modem, it can be passed via the cPCI backplane boards in the chassis (e.g., power control output messages) or to other parts of the s higher-level protocol processing or distribution. In the **Figure 2**, the data was passed to board computer (SBC), which acted both as a host for all the cards in the rack as gateway to a terrestrial packet network.

COTS-Custom combination solution

Due to flexibility built into the baseboard, other architectures can be considered in cas the existing COTS interfaces do not meet all of the specifications required. The reason as simple as a requirement to avoid front panel cabling, or it might be motivat communications channel issue such as signal-to-noise-ratio concerns arising from parti of the multiple access environment. For instance, this could occur where there is a lar difference (e.g., 20dB) between carriers. Such a difference might result in Ka-band where one terminal's transmission is attenuated by precipitation [10] while another is not. IF bandwidth is digitized all at once in the presence of these power differences, the resul of over 3 significant bits (for 20dB) in the digitization of the less powerful signals (since input must be scaled to handle the largest signals to avoid saturation). Another cas custom solutions may be required is when carrier density is high in the presence of bandwidth. In this situation, digitization of the IF by the A/D may suffer from significant of intermodulation distortion (IMD).

IMD arises from nonlinearities in the A/D converter. The nonlinearities result in the for harmonics and distortion components at sums and products of the carrier frequencies. in **Figure 4,** when digitizing two carriers, f1 and f2, distortion products arise at 2f1, 2f2, f2, 2f1+f2, 2f2+f1, 2f1-f2, 2f2-f1, etc. Some of these distortion components are far from th of interest, such as f1+f2, and can be removed by filtering. Others fall near the themselves, such as the third-order products, 2f1-f2, and 2f2-f1. In the presence of more there are correspondingly more distortion components generated (from all the possible p leading to even more IMD. The increasing noise floor reduces the effective number resolution in the digitized signal.
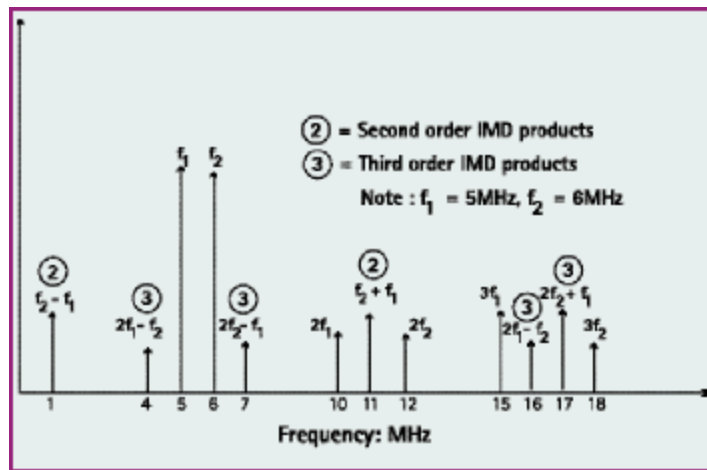
Figure 4: Intermodulation Distortion effects (IMD) [From: Analog Devices Seminar, "Section 4 – High Speed Sampling ADCs," Walter Kester, found at www.analog.com/support/standard_linear/seminar_material/practical_ design_techniques/practical_design.html]

Note that a custom SDR solution is not necessarily required to address the IMD described in the previous paragraphs. The standard COTS solutions can still be a narrower-band analog downconverters are employed at the RF stage, resulting in a band IF input into the SDR subsystem.

Regardless of the impetus, COTS systems often have the flexibility to integrate custom into the solution. For instance, with the cPCI baseboard that we discussed previou integration could take the form of custom mezzanine modules on the baseboard's PE PMC sites. In addition, a cPCI transition module can be connected to the cPCI J5 con the back of the cPCI backplane.

As shown in **Figure 5**, the PMC connector known as the user-defined connector (as spec) is routed to the user-defined J5 connector on the cPCI backplane. The trace connector on the baseboard have been optimally routed and impedance balanced to giv quality signal interface. The transition module on the back of the chassis interfaces connector and injects signals through the backplane, into the user-defined PMC conne the baseboard, a custom designed mezzanine module covering both the PMC and the F would be used to format and transfer the data to the individual PEM connectors of ea processors.
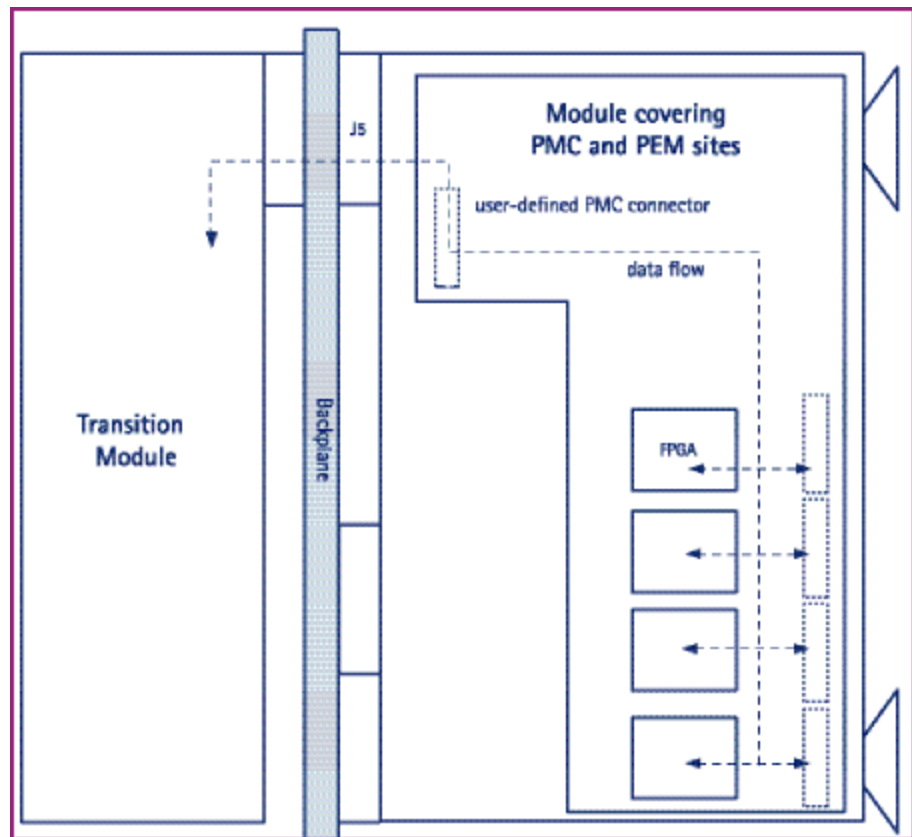
Figure 5: Custom-COTS system using backplane transition module

Note that while the primary purpose of the mezzanine board discussed in the previous p
is to translate and route signals from the backplane to the processor PEM bus, one c
advantage of the mezzanine space, and place FPGAs on the mezzanine. These FPG
function as co-processors, performing some of the functions discussed earlier.

Future Directions/ Challenges
The future SDR architectures for satellite earth stations are being shaped by an inters
requirements from physics, customer expectations (QoS), and technological progres
building blocks of SDR.

Physics
The relatively wide bandwidths involved in satcom (18 MHz, 29 MHz, 36 MHz), couplec
increasing number of carriers required to handle growing data traffic, create a hurdle
because of intermodulation distortion, as discussed earlier. Until A/D's can be crea
sufficiently high resolution and linearity to produce low IMD specs, some applications
require analog IF filters to divide the wide bandwidth into smaller chunks before digitiz
place. The problem of unequal power carriers, discussed earlier will also become less s
as A/D resolution improves.

Customer Expectations (QoS)
Today, businesses are extremely dependent on their computer networks. When the
crashes, it's no longer just a few employees who are left hanging -- it's virtually ever
collaboration among remote offices continues and business travel increases, the expec
rather demand, for reliable broadband connectivity surges. Since even the most reliable
do occasionally break down or require maintenance, this leads to the concept of fault tol
n-times-redundant systems. The advent of hot-swap has addressed this now, but the
architectures are generally still at risk for single-point failures by the SBC host (e.g., bec
a single-point gateway or simply due to its role in hosting the cPCI bus). Therefore, futu
boards will need to have the ability to self-host and act as their own gateway to th

network, or a distributed hosting will be required.

Technological Progress

FPGA capability is increasing dramatically all of the time. FPGAs are now strongly challe
role of ASICs, and even displacing them in some cases a trend that will accelerate in t
The parallel buses currently used on backplanes (e.g., VME, cPCI) are giving way to
schemes and Ethernet. Overall, this concept of the cPCI packet-switched backplane
greater throughput on the backplane, eliminating current bottlenecks in inter-board data t

Open software standards like CORBA are emerging to reduce code development c
expanding the offerings of compatible algorithm libraries and ensuring portability of the
new hardware platforms with minimum re-work. Together, these technologies, and ot
shape the look of future SDR platforms for satellite systems.

Summary

Satellite communication is growing in popularity and finding its way into more co
residences, and even individuals' pockets as an avenue for telephony, high-speed
access, and data network connectivity. As the number of users increases and the d
climb, new technologies must be applied to increase channel densities and throug
standards evolve and requirements change, so does the need to evolve and imp
infrastructure equipment. Software defined radio provides an ideal path on which to
evolution. Today's COTS platforms can take care of the SDR implementation details, all
infrastructure OEMs to focus their efforts on the product differentiators that add customer

[1] Even though the processor discussed above are often executing more than one instru
given clock cycle, there is still a fetch-and-execute scheme taking place

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